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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,745	07/21/2000	KARL AMUNDSON	INK-086-(2108/66)	4716

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EXAMINER
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NGUYEN, JIMMY H

ART UNIT	PAPER NUMBER
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2673

13

DATE MAILED: 01/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/621,745

Applicant(s)

AMUNDSON ET AL.

Examiner

Jimmy H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 October 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3,7-12,15,16 and 18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3, 7-12,15,16 and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 10/20/2003 (entered into the file wrapper as Paper No. 12). Claims 1, 3, 7-12, 15, 16 and 18 are currently pending in the application. An action follows below:

#### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 7-12, 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hopper et al. (the C1 reference cited in IDS filed on 02/05/2001), hereinafter Hopper, in view of Oversluizen et al (USPN: 6,100,951), hereinafter Oversluizen, and further in view of Morin et al (USPN: 5,238,861, cited in IDS filed on 02/05/2001), hereinafter Morin.

As per claims 1 and 18, Hopper discloses an electrophoretic display (see Title) comprising a display medium (a contrasting medium, page 1148, second column, line 6, fig. 6) comprising at least one capsule (a cell, fig. 6, page 1149, first column, line 5, second column, last paragraph, lines 6-8) containing a plurality of electrophoretic particles dispersed in a fluid medium (page 1148, second column, lines 5-7), a transistor (a TFT, fig. 5) including a data line (a source electrode, fig. 5), a gate electrode (a gate electrode, fig. 5) and a pixel electrode (fig. 5), and a storage capacitor (Cs) (fig. 5). Hopper further teaches that the particles move during evolution of an optical state of the display medium (fig. 3 and Addressing Section on page 1151). Accordingly, Hopper discloses everything except for a layer of insulating material and the first

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and second layers of the transistor and a layer of insulating material, the first and second layers of conductive material of the storage capacitor, as recited in independent claims 1 and 18 above.

However, Oversluizen discloses a related electrophoretic display (col. 1, lines 21-23 and col. 5, lines 31-33) comprising a transistor (a TFT, see fig. 21, col. 8, lines 36-39) including a layer of insulating material (a layer of insulating material 62, col. 9, line 30) and a layer of semiconducting material (42') (see fig. 21, col. 8, line 58), both situated between a first layer of conductive material (17,57) and a second layer of conductive material (16, 18, 18a, 56, 58, 66) (see col. 8, lines 32-36); and a storage capacitor (Cs) (see fig. 21, col. 9, lines 30-33) including a layer of insulating material (a layer of insulating material 62, see col. 9, line 30) situated between a first layer of conductive material (17,57) and a second layer of conductive material (16, 18, 18a, 56, 58, 66) (see col. 8, lines 32-36). Oversluizen further teaches that with the structures of the transistor and the storage capacitor as discussed above, the display device can be manufactured in a simple and inexpensive manner and have advantageous characteristics (abstract and col. 2, lines 2-5). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to provide the specific structures of the transistor and the storage capacitor, as discussed above and as taught by Oversluizen, in the device of Hopper because this would provide a user an inexpensive display device with a better quality, as taught by Oversluizen (abstract and col. 2, lines 2-5).

However, the combination of Oversluizen and Hopper teaches the transistor comprising a layer of the patterned semiconducting material (42') situated between the respective first layer of conductive material and the respective second layer of conductive material, but does not expressly teach that the transistor and the storage capacitor share a single layer of unpatterned

change to 42 being a layer of patterned material or unpatterned, as claimed.

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semiconducting material situated between the respective first layers of conductive material and the respective second layers of conductive material, as recited in claim 1, or the storage capacitor comprising a layer of unpatterned semiconducting material situated between the first layer of conductive material and the second layer of conductive material, as recited in claim 18.

However, Morin discloses an active matrix display device (figs. 4a and 4b) comprising a transistor (a TFT, see fig. 4a, col. 4, line 1) and a storage capacitor (Cs) (see fig. 21, col. 4, line 8), both sharing a single layer (semiconductive film 14, col. 5, line 1) of unpatterned semiconducting material and a single layer (non-conducting film 16, col. 5, lines 1-2) of insulating material, both situated between the respective first layers (a conductive film 18, col. 5, line 2) of conductive material and the respective second layers (12, P) of conductive material (col. 3, lines 46-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to substitute Morin's the layer of unpatterned semiconducting material for the layer of patterned semiconducting material in the system of Hopper in view Oversluizen, because this would reduce the complexity of manufacturing the system, as taught by Morin (col. 2, lines 41-43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to combine Morin and Oversluizen with Hopper to obtain the invention defined in claims 1 and 18.

Regarding to claims 3 and 12, Oversluizen further discloses that the layer of insulating material of the transistor and the layer of insulating material of the storage capacitor are the same continuous layer of insulating material (62) (see fig. 21), and Morin also discloses that the layer of insulating material of the transistor and the layer of insulating material of the storage capacitor are the same continuous layer of insulating material (16) (see figs. 4a and 4b).

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Morin  
in  
design  
from

Regarding to claims 7 and 8, Oversluizen further discloses that the storage capacitor is in electrical communication with a neighbouring gate electrode (57) (i.e., the claimed second gate line of claim 7 or the claimed conductor of claim 8).

Regarding to claim 9, Oversluizen further discloses that the second layer (16, 18, 18a, 56, 58, 66) of conductive material of the storage capacitor forms a storage capacitor pixel electrode (18a) and the first layer (17, 57) of conductive material of the storage capacitor forms a storage capacitor gate electrode (57) (see fig. 21).

Regarding to claim 10, Oversluizen further discloses that the layer of insulating material of the storage capacitor is patterned (col. 3, lines 34-40).

Regarding to claim 11, Oversluizen further discloses that the layer (62) of insulating material of the storage capacitor is unpatterned (see fig. 21).

Regarding to claim 15, Hopper discloses expressly that the capacitance of the storage capacitor ( $C_s = 1.5 \text{ pF}$ ) is greater than the capacitance of a pixel ( $C_{EF} = 0.055 \text{ pF}$ ) (page 1151, second column).

Regarding to claim 16, Hopper further teaches that the capacitance of a pixel exists (fig. 5), and Oversluizen discloses that an inherent capacitance (C) of the pixel and an inherent resistance (R) of the pixel exist (col. 10, lines 1-11). Accordingly, one skilled in the art at the time of the invention was made would recognize that, in the presence of the storage capacitor ( $C_s$ ), the voltage decay time across the pixel is based on the product of R and  $(C + C_s)$  (since C and  $C_s$  are parallel in connection).

### ***Response to Arguments***

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4. Applicant's arguments with respect to independent claims 1 and 18 have been considered but are moot in view of the new ground(s) of rejection. Please see the new ground(s) of rejection above.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is (703) 306-5422. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at (703) 305-4938.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

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Washington, D.C. 20231

**or faxed to:**


**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,  
Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding  
should be directed to the Technology Center 2600 Customer Service Office whose telephone  
number is (703) 306-0377.

JHN

January 6, 2004

  
BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600